別紙５（論文博士）

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Department: 電気・電子情報工 学専攻			
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Abstract
論文内容の要旨（博士）

Title of Thesis 博士学位論文名	半導体デバイスバックエンドプロセスの複合要因故障と故障解析技術

(Approx. 800 words)
(要旨　1,200 字程度)

市場環境の変化や商品の多様化・小型化に伴い、これまで予想できなかった新たな複合要因による磨耗故障モードによる信頼性上の問題が発生しつつある。これらの新たな複合要因による磨耗故障モードとは、設計と製造プロセスの複数工程に関連した複合的な故障モードであり、それらの関連性を理解し、緻密な故障解析から発生原因、故障メカニズムを明らかにしたうえで、正しい再発防止に結び付ける必要がある。

本研究では、wafer level chip size package デバイス搭載のモジュール製品の開封技術、裏面 photon emission microscope 発光解析用 Si 基板の薄膜化技術などの新たな故障解析技術を開発し、ソフトウェアによる故障箇所特定精度を検証した。これらの技術を用いて anti-refraction coating-TiN 膜腐食、Via の高抵抗化、層間 TEOS 酸化膜クラック、Al 膜中のボイド等の複合的要因による磨耗故障モードについてその発生原因と故障メカニズムを明らかにした。

初めに、第 1 章序論では、本研究の背景と目的、半導体デバイスの故障解析、故障解析技術の分類について述べる。

その後、第 2 と第 3 章では、故障解析技術について述べる。まず、第 2 章では、電気化学的エッチング技術を用いた wafer level chip size package n-型 Si デバイス搭載のモジュール製品の開封技術について述べる。DC 電圧を印加しながら KOH アルカリ水溶液を用いるもので、Si 基板の KOH によるエッチングを電気化学的作用で防止する。次に第 3 章では、optical band pass filter を用いる発光スペクトル解析と印加電圧に伴なう発光数の累乗近似式から、半導体デバイスの代表的な故障モードの推定精度を向上させた。更に、発光解析で特定された故障箇所の Si 基板裏面からの発光スペクトル解析の為、ダメージの無い任意箇所の Si 基板薄膜化技術を開発した。

第 4 章から第 6 章までは、複合要因による故障メカニズムについて述べる。まず、第 4 章では、TiN/Al-1%Si-0.5%Cu / anti-refraction coating-TiN の積層配線構造におけるボイド形成の原因を調査し、下層バリヤ Ti 膜の窒化処理温度、上層 tetraethyl orthosilicate 酸化膜の特性から、下層バリヤ TiN 膜と上層 tetraethyl orthosilicate 酸化膜の複合要因によるボイド形成のメカニズムを明らかにした。第 5 章では、tetraethyl orthosilicate 酸化膜や spin-on-glass 酸化膜クラック後の内部残留水分拡散と印加電圧による anti-refraction coating -TiN 膜腐の原因となるクラックは、tetraethyl orthosilicate 酸化膜の低屈折率化と大面積の上層メタル配線端部の spin-on-glass 酸化膜上の位置関係が原因で発生し、これらの複合要因による故

障である事を明らかにした。更に、anti-refraction Coating -TiN 膜の腐食部でのフッ素検出は、膜密度が低下した TiON 膜中をフッ素が拡散し、下層の Al 配線と反応したものが energy dispersive X-ray spectrometry 分析で検出されたものであった。更に 6 章では、Via 高抵抗メカニズムを調査し、設計とプロセスの相互要因が原因である事を明らかにした。メタル配線レイアウトと Via 位置の複合要因が、via 内部の Ti_xAl_y 合金層とボイド形成に影響していた。

第7章は、今後の故障解析技術として、ソフトウェアを用いた故障診断技術による故障箇所特定の精度を評価し、高い精度で故障箇所を特定できる事が分った。ソフトウェアによる故障箇所特定精度は高いが、従来のphoton emission microscope解析やoptical beam induced resistance change 解析との併用が精度向上に必要である事を示した。

最後の 8 章では、今後の最先端デバイスと既存デバイスの故障解析技術ついて述べたる。

以上の様に、半導体デバイスの故障モードは多様化・複雑化しており、故障現象から単純に従来の故障モードに当てはめて対策を講じることは何ら問題の解決にならず、複雑な複合要因による磨耗故障モードを念頭においた故障解析が必要である。

別紙５（論文博士）

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Department: Electrical and Electronic Information Engineering			
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Abstract

論文内容の要旨（博士）

Title of Thesis 博士学位論文名	Backend process multifactor failure mechanism and failure analysis technique of semiconductor devices

(Approx. 800 words)

(要旨　1,200字程度)

The increasingly fast-changing market environment has created new, unexpected modes of wear-out failure by multifactor, which can lead to reliability issues. These new, unexpected modes of wear-out failure by multifactor are related to circuit design, layout design, and manufacturing. Deep failure analysis is necessary to clarify the cause of wear-out failure by multifactor, understand its mechanism, and prevent it from recurring.

In this study, we examined failure analysis techniques for new devices. These include a decapsulation technique for wafer level chip size package module devices, random location damage-free Si substrate thinning technique for the Si substrate backside photon emission microscope analysis, and a software fault localization technique, which we compared with conventional hardware techniques in terms of accuracy. We determined the multifactor failure causes and mechanisms for the corrosion of an anti-refraction coating-TiN film, via high resistance, tetraethyl orthosilicate-oxide film cracking, and metal line voids though several related processes.

In section 2, We developed an electrochemical etching technique to decapsulate the overcoated anhydride cured on the epoxy resin. The method uses a KOH alkali solution with DC bias voltage applied to a wafer level chip size package n-type Si device. The DC bias acts as an electrical-etch-stopper of the n-type Si device's substrate during the decapsulation of the overcoated resin. The efficiency and effectiveness of our decapsulation technique were evaluated using a Li ion/polymer protector module device.

In section 3, we found that emission spectral analysis using an optical band pass filter was effective for estimating the mode of failure for semiconductor devices. Furthermore, we could estimate the failure mode, including the metal/metal line short mode, from the following power approximation formula: $Y = aX^b$ of the photon count increase rate under photon emission microscope observation. These two techniques allow for much more precise estimations of the representative failure modes of semiconductor devices. Next, we developed a damage-free, large-area local Si substrate thinning technique for backside photon emission spectral analysis at an isolated point. We succeeded in estimating the failure mode of semiconductor devices by backside photon emission spectral analysis using these techniques.

In section 4, we investigated the void formation mechanism in a TiN/Al-1%Si-0.5%Cu/anti-refraction

coating-TiN multilayer structure. The nitriding processing temperature of the underlayer barrier Ti film and the characteristics of the upper plasma enhanced Tetraethyl orthosilicate SiO2 film had evident effects on the void formation mechanism. We will demonstrate the formation process of a new void.

In section 5, we investigated the corrosion of the anti-refraction coating-TiN film (TiO_xN_y-oxidation) in semiconductor devices due to residual moisture after a crack is generated in the tetraethyl orthosilicate-oxide or spin-on-glass SiO_2 film. We examined both metal line layout and tetraethyl orthosilicate-oxide film characteristics. The root causes of cracking were the low refractive index of the cap-tetraethyl orthosilicate-oxide film and the wide, long metal2 edge location on the spin-on-glass SiO_2 film. Next, we examined the cause of the fluorine detected during the corrosion of the anti-refraction coating-TiN film. More specifically, energy dispersive X-ray spectrometry analysis detected that fluorine reacted with the Al line in the underlying layer after diffusing through the porous TiO_xN_y film.

In section 6, we investigated the root cause of a via high resistance issue due to fabrication process variations and mismatching design rules. The analyses revealed the root cause as the formation of a Ti_xAl_y layer with small, porous void areas around the failed via bottom due to poor step coverage of the TiN/Ti barrier layer. Next, design rule analysis indicated that the via high resistance issue tends to occur only at high-driver cells with many fan-outs. From these combined analyses of fabrication and design, we found that metal1 layout and the location of the via on metal1 influence Ti_xAl_y and void formation. Metal line design rule is thus strongly related to this via high resistance issue.

In section 7, we verified the accuracy of failure localization by a software-based fault diagnosis technique through comparison with failure localization by photon emission microscope analysis and optical beam induced resistance change analysis. We found that the software technique could accurately localize the failure with a high probability (85.7%). Although software-based fault diagnosis is a powerful tool for failure localization, it must be combined with hardware techniques such as Photon emission microscope analysis and optical beam induced resistance change analysis to maintain its accuracy.

In section 8, we consider the future of failure analysis technology for both cutting-edge and old design devices, and we consider the skills, qualities, and abilities a technician must have to conduct failure analysis on both types of semiconductor devices.

As described above, the interdependency of circuit design, layout design, and manufacturing has become increasingly important for semiconductor device reliability. Because the failure modes of semiconductor devices have also become increasingly complicated, reliability problems can often not be solved by finding a conventional single failure mode for a failure phenomenon. Failure analysis engineers should conduct failure analyses in consideration of complex failure modes. The reliability of next-generation semiconductor devices can only be improved by fundamental measures and improvements resulting from the investigation of complex wear-out failure mode by multifactor and causes.